iU6398

3-Phase BLDC Motor Controller

Datasheet Rev. 0.1 (Preliminary version, not MP version)

1. Description

The iU6398 is a 3-phase BLDC motor controller IC integrated with various peripherals to realize sensor or sensor-less BLDC motors application, including FOC. The iU6398 is embedded with 3-phase N/N MOS pre-driver and HV-BUCK controller. The logic input is compatible with standard CMOS output. It features the flexibility to adjust various motor parameters and complete protection such as over current, over voltage and under voltage lockout.

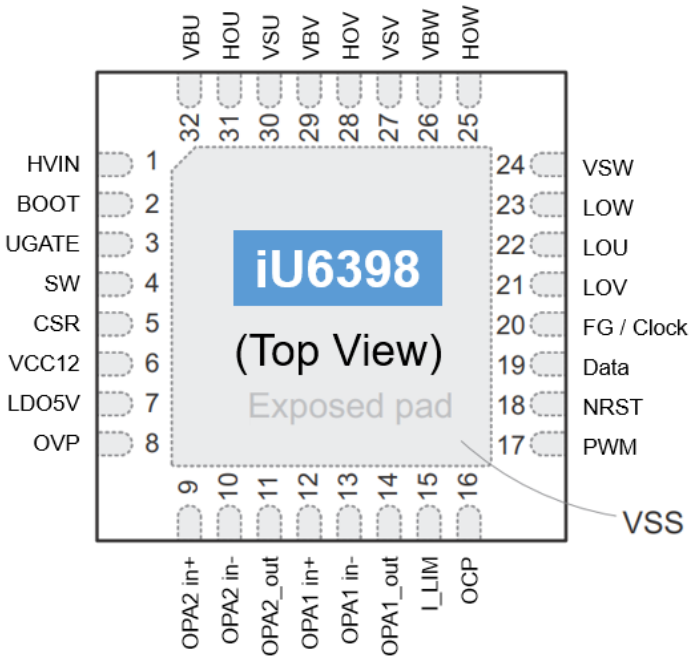
2. Features

- 3-Phase BLDC Motor Controller with pre-driver and HV-BUCK controller
- Embedded 3-phase N/N MOS Pre-driver with Maximum voltage up to 160V
- Embedded HV-BUCK Operating Supply Voltage up to 80V
- Integrated Current Amplifier x 2
- Programmable Locked Rotor and Restart Timing
- Programmable Soft Start Timing
- Complete Protection such as OCP/OVP/UVLO
- QFN-32 4x4 Package

3. Applications

- BLDC Motor Driver (12~96V)

4. Pin Assignments



5. Marking Information

Product Name	Marking
iU6398	 X: Date code

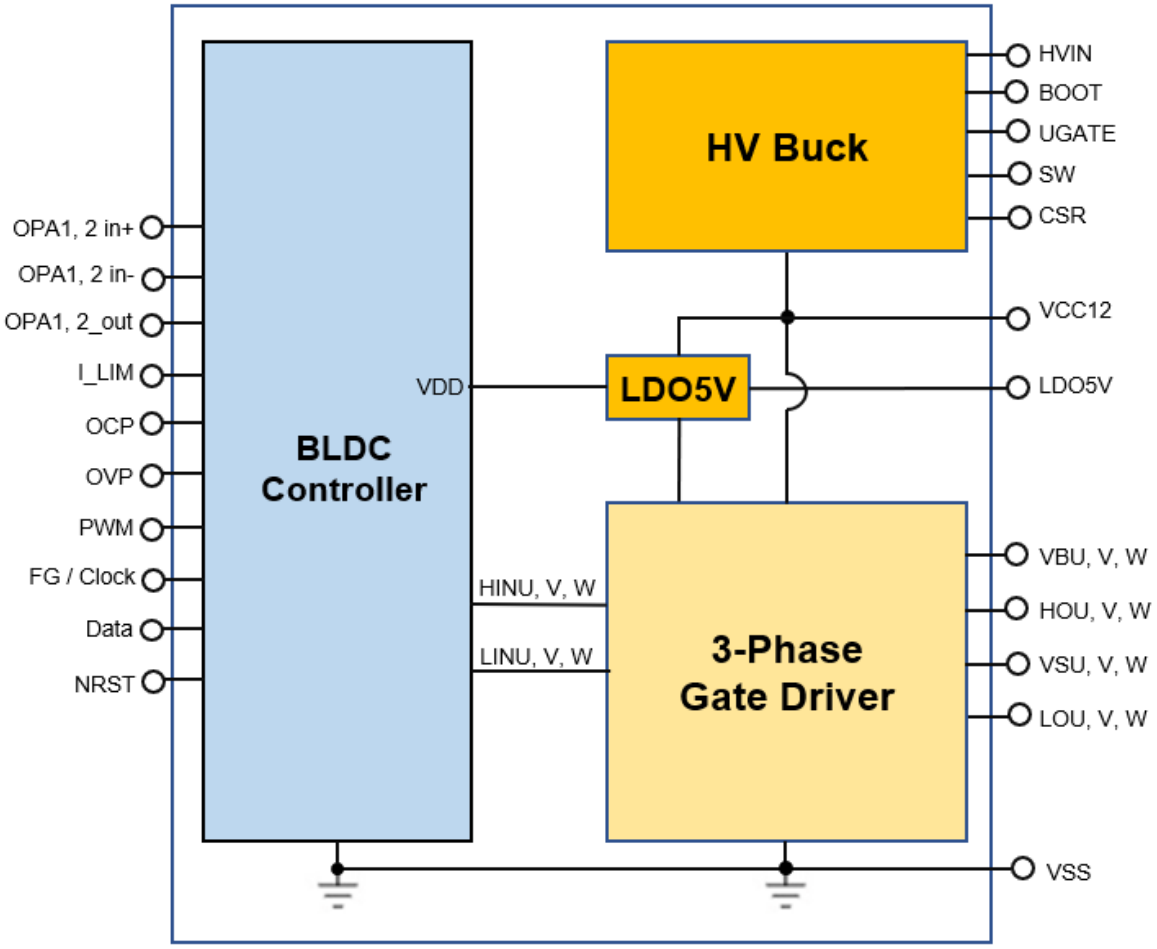
6. Ordering Code

Ordering Code
iU6398

7. Pin Definitions

Pin No.	Symbol	Description
1	HVIN	HV Buck Power Input
2	BOOT	Bootstrap Voltage to HV-BUCK High-side Gate Driver
3	UGATE	HV Buck High-side Gate Control
4	SW	HV Buck Switch Node
5	CSR	HV Buck Current Sensor
6	VCC12	12V Power Supply
7	LDO5V	5V LDO Output
8	OVP	Over Voltage Protection
9	OPA2 in+	OPAMP2 Positive Input
10	OPA2 in-	OPAMP2 Negative Input
11	OPA2_out	OPAMP2 Output
12	OPA1 in+	OPAMP1 Positive Input
13	OPA1 in-	OPAMP1 Negative Input
14	OPA1_out	OPAM1 Output
15	I_LIM	Average Current Detection
16	OCP	Over Current Protection
17	PWM	PWM Input
18	NRST	External RESET
19	Data	Data Input
20	FG / Clock	FG / Clock Input
21	LOV	V-Phase, Low Side Gate Driver
22	LOU	U-Phase, Low Side Gate Driver
23	LOW	W-Phase, Low Side Gate Driver
24	VSW	W-Phase, Power Switching Output Node
25	HOW	W-Phase, High Side Gate Driver
26	VBW	W-Phase, Bootstrap Power Supply
27	VSV	V-Phase, Power Switching Output Node
28	HOV	V-Phase, High Side Gate Driver
29	VBV	V-Phase, Bootstrap Power Supply
30	VSU	U-Phase, Power Switching Output Node
31	HOU	U-Phase, High Side Gate Driver
32	VBU	U-Phase, Bootstrap Power Supply
EP	VSS	Ground

8. Function Block Diagram



9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Unit
VCC12	Voltage of LDO and Gate Driver Supply Input	-0.3	20	V
LDO5V	Voltage of LDO Output	-0.3	5.8	V
VHO1,2,3	Voltage of High Side Gate Driver Output	VS - 0.3	VB + 0.3	V
VLO1,2,3	Voltage of Low Side Gate Driver Output	-0.3	VCC12 + 0.3	V
VB1,2,3	Bootstrap Voltage to High Side Gate Driver	VS - 0.3	VS + 20	V
VS1,2,3	Voltage of Return Path for High Side Gate Driver	-0.3	160	V
VHIN	Voltage of HV-BUCK Power Input	-0.3	100	V
VSW	Voltage of HV-BUCK Phase Switch	-0.3	100	V
VGATE	Voltage of HV-BUCK High Side NMOS Gate	VSW-0.3	VBOOT+0.3	V
VBOOT	Voltage of HV-BUCK BOOT Pin	VSW-0.3	VSW+VCC12	V
VCS	Voltage of HV-BUCK Over Current Detect	VCC-1V	VCC+1V	V
dVS/dt	VS Voltage Slew Rate	--	50	V/ns
I/O Pin	Logic Input Voltage	- 0.3	5.55	V
Tj	Junction Temperature (Note)	-40	125	℃
T_S	Storage Temperature	-55	150	

Note: Please do not exceed Tj limitation

In the following electrical characteristics, the parameter given in the table below is derived from the tests performed under general operation conditions and room temperature, unless special bias or temperature condition is specified.

9.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
VCC12	Voltage of LDO and Gate Driver Supply Input	5.5	16	V
LDO5V	Voltage of LDO Output	4.75	5.25	V
VHO1,2,3	Voltage of High Side Gate Driver Output	VS	VB	V
VLO1,2,3	Voltage of Low Side Gate Driver Output	0	VCC12	V
VB1,2,3	Bootstrap Voltage to High-side Gate Driver	VS - 0.3	VS + VCC12	V
VS1,2,3	Voltage of Return Path for High Side Gate Driver	-9*	120	V
VHIN	Voltage of HV-BUCK Power Input	20	80	V
VSW	Voltage of HV-BUCK Phase Switch Node	0	80	V
VGATE	Voltage of HV-BUCK High Side NMOS Gate	VSW	VBOOT	V
VBOOT	Voltage of HV-BUCK BOOT Pin	VSW+5V	VSW+VCC12	V
VCS	Voltage of HV-BUCK Over Current Detect	VCC-0.8V	VCC+0.8V	V
I/O Pin	Logic Input Voltage	0	5.3	V
T_A	Ambient Temperature (Note)	-40	105	℃

Note: Please do not exceed Tj limitation

*: Not DC level, only pulse condition and pulse width less than 10us.

9.3 D.C. Characteristics

Symbol	Conditions			Min.	Typ.	Max	Unit
	Mode	f_{HCLK}	Conditions				
IDD*	Operation Mode Internal Clock	60MHz	All Peripherals Enabled	-	8.61	-	mA
			All Peripherals Disabled	-	7.08	-	mA
		40KHz	All Peripherals Enabled	-	1.02	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Sleep Mode, Internal Clock	60MHz	All Peripherals Enabled	-	3.52	-	mA
			All Peripherals Disabled	-	2.25	-	mA
		40KHz	All Peripherals Enabled	-	1.00	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Stop Mode	-	Enter Stop Mode after Reset	-	110	-	uA

* Only BLDC controller. HV-Buck and Gate Driver are not included.

9.4 A.C. Characteristics

9.4.1 High Speed Internal Oscillator (HSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
f_{HSI}	Frequency	-	-	60	-	MHz
ACC_{HSI}	Accuracy of HSI Oscillator	T_A = -40°C ~ 105°C	-2.5	-	+2.5	%
		T_A = -10°C ~ 85°C	-1.5	-	+1.5	%
		T_A = 25°C	-1	-	+1	%

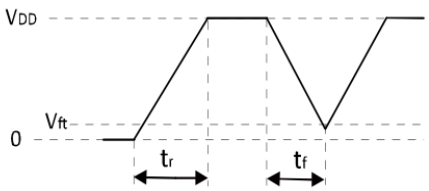
9.4.2 Low Speed Internal Oscillator (LSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
F_{LSI}	Frequency	T_A = -40°C ~ 105°C	20	40	60	KHz
$tsu_{(LSI)}$	LSI Oscillator Start-up Time	-	-	-	300	us
$IDD_{(LSI)}$	Power Consumption of LSI Oscillator	-	-	0.34	-	uA

9.4.3 Power-up and Power-down Characteristics

Symbol	Conditions	Min.	Typ.	Max	Unit
t_{VDD}	VDD Rising Time tr	300	-	50000	us
	VDD Falling Time tf	300	-	50000	
V_{ft}	Power-down Threshold Voltage	0	-	-	mV

Note 1：Derived from overall evaluation, not tested in production.
Note 2：The on-chip VDD waveform during power-down should follow the tr and tf stages as shown in the waveform diagram below.
Note 3：The chip should be powered up from 0V to ensure reliable power-up.
Note 4：VDD means LDO5V for BLDC controller power supply.



9.4.4 Low-Power Mode Wake-up Time

Symbol	Conditions	Min.	Typ.	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep Mode (System Clock is HSI)	-	1.5	-	us
t_{WUSTOP}	Wake-up from Stop Mode (System Clock is HSI)	-	65	-	us

9.5 Input / Output Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{IL}	Input low-level voltage	5V CMOS port	-	-	0.3 * VDD	V
V_{IH}	Input high-level voltage	5V CMOS port	0.7 * VDD	-	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	5V	0.1 * VDD	0.60	-	V
I_{lkg}	Input leakage current	5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	Vinput= VSS	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor	Vinput= 5V	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

Note：VDD means LDO5V for BLDC controller power supply.

Symbol	Parameter	Conditions	Typ.	Unit
V_{OL}	Output low level	$\|I_{IO}\|$ = 6mA，VDD = 5V	0.11	V
V_{OH}	Output high level		4.83	
V_{OL}	Output low level	$\|I_{IO}\|$ = 8mA，VDD = 5V	0.15	
V_{OH}	Output high level		4.78	
V_{OL}	Output low level	$\|I_{IO}\|$ = 20mA，VDD = 5V	0.38	
V_{OH}	Output high level		4.4	

Note：VDD means LDO5V for BLDC controller power supply.

9.6 POR / PVD Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{PVD}	Level Selection for Programmable Voltage Detector	Rising Edge: Level 1	-	2.4	-	V
		Falling Edge: Level 1	-	2.3	-	V
		Rising Edge: Level 2	-	2.7	-	V
		Falling Edge: Level 2	-	2.6	-	V
		Rising Edge: Level 3	-	3.0	-	V
		Falling Edge: Level 3	-	2.9	-	V
		Rising Edge: Level 4	-	3.3	-	V
		Falling Edge: Level 4	-	3.2	-	V
		Rising Edge: Level 5	-	3.6	-	V
		Falling Edge: Level 5	-	3.5	-	V
		Rising Edge: Level 6	-	3.9	-	V
		Falling Edge: Level 6	-	3.8	-	V
		Rising Edge: Level 7	-	4.2	-	V
		Falling Edge: Level 7	-	4.1	-	V
		Rising Edge: Level 8	-	4.5	-	V
		Falling Edge: Level 8	-	4.4	-	V
		Rising Edge: Level 9	-	4.8	-	V
		Falling Edge: Level 9	-	4.7	-	V
V_{POR}	Power-on Reset Threshold	-	-	2.2	-	V
$V_{hyst\_POR/PDR}$	POR/PDR Hysteresis	-	-	60	-	mV
$T_{RSTTEMPO}$	Reset Duration	-	-	1.84	-	ms

9.7 A/D Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
f_{ADC}	ADC Clock Frequency	VDD ≥ 2.5V	-	-	15	MHz
f_S	Sampling Rate	12bits; VDD ≥ 2.5V	-	-	1	MHz
f_{TRIG}	External trigger frequency	12bits; f_{ADC} = 15MHz	-	-	1	MHz
		12bits	-	-	15	1/ fADC
R_{AIN}	External Input Impedance	-	See the formula below			KΩ
R_{ADC}	Sampling switch resistance	-	-	-	1.5	KΩ
C_{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
t_{STAB}	Power-up Time	-	-	-	10	μS
t_{lat}	Injection-Trigger Conversion Delay	-	-	-	512	1/fADC
t_{latr}	Regular-Trigger Conversion Delay	-	-	-	512	1/fADC
ts	Sampling Time	f_{ADC} = 15MHz	0.167	-	16.03	μS
t_{CONV}	Total Conversion Time (including Sampling Time)	12bits; f_{ADC}=15MHz	1	-	16.87	μS
ENOB	Effective Number of Bits	12bits; VDD ≥ 3.3V; f_{ADC} = 15MHz	-	10.9	-	bit

Note 1：For external triggering, a delay of 1/f_{ADC} must be added to the timing

Note 2：VDD means LDO5V for BLDC controller power supply.

Symbol	Parameter	Conditions	Typ.	Unit
ET	Overall Error	f_{PCLK1}=60MHz, f_{ADC}=15MHz, R_{AIN}<0.1KΩ, VDD=5V, T_A=25°C	-4.7 to +3.4	LSB
EO	Offset Error		-1.9 to +2.8	LSB
EG	Gain Error		-0.4 to +1.6	LSB
ED	Differential Linearity Error		-1.0 to +0.4	LSB
EL	Integral Linearity Error		-2.2 to +3.4	LSB

Note：VDD means LDO5V for BLDC controller power supply.

9.8 Operational Amplifier Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{DD}	Supply Voltage	-	2.5	-	5.5	V
V_{OFFSET}	Input Bias Voltage	-	-	1	-	mV
I_{LOAD}	Drive Current	Drive current (sinking current) (VDD=5V, VOUT=1V)	-	-	15	mA
C_{LOAD}	Capacitive Load	-	-	-	30	pF
CMRR	Common Mode Rejection Ratio	-	-	80	-	dB
PSRR	Power Supply Rejection Ratio	-	-	80	-	dB
GBW	Gain-Bandwidth Product	-	-	12	-	MHz
SR	Slew Rate	-	-	7	-	V/us
GOL	Open-loop Gain	-	90	110	120	dB

Note: VDD means LDO5V for BLDC controller power supply.

9.9 Comparator Electrical Characteristics

Symbol	Parameter	Register Configuration	Min.	Typ.	Max	Unit
t_{HYST}	Hysteresis	00(hysteresis), high power	-	0	-	mV
		00(hysteresis), low power	-	0	-	mV
		01(hysteresis), high power	15	22	43	mV
		01(hysteresis), low power	13	15	23	mV
		10(hysteresis), high power	32	45	92	mV
		10(hysteresis), low power	25.2	32	46.7	mV
		11(hysteresis), high power	55	85	182	mV
		11(hysteresis), low power	25.5	60	83.9	mV
V_{OFFSET}	Offset Voltage	-		+/-6	+/-10.4	mV
t_{DELAY}	Propagation Delay Note1	00（high power）	3.7	10.7	43	ns
		01（medium power）	10.5	34.9	83	ns
		10（low power）	13.8	49	114	ns
		11（ultra-low power）	22.2	86	194.5	ns
Iq	Average Operating Current	00（high power）	6.5	45	205.4	μA
		01（medium power）	3.3	21.7	81.3	μA
		10（low power）	2.6	15.3	59.6	μA
		11（ultra-low power）	1.7	8.8	35.3	μA

Note1 : Time difference between 50% output transition and input transition.

9.10 Gate-driver Electrical Characteristics

(Ta = 25°C, VCC12 = VBS = 12V, Cload = 1000pF)

Symbol	Description	MIN	TYP	MAX	Unit
Dynamic Parameters					
ton	Turn-on Delay Time	-	150	300	ns
toff	Turn-off Delay Time	-	150	300	ns
tr	Rising Time	-	40	60	ns
tf	Falling Time	-	15	30	ns
MTon	Matching Turn-on Delay Time	-	20	50	ns
MToff	Matching Turn-off Delay Time	-	40	80	ns
tPM	PWM Pulse Matching Time	-	50	75	ns
tDT	Dead Time	200	300	400	ns
Static Parameters					
VOH	High Level Output Voltage, IO=-20mA	-	-	VCC12 - 0.3	V
VOL	Low Level Output Voltage, IO=20mA	-	-	0.2	V
IQCC	VCC Quiescent Current, HO&LO=Low	-	-	0.8	mA
IQBS	$VB_{1,2,3}$ Quiescent Current, HO=Low	-	30	60	uA
ILK	VS Leakage Current	-	-	10	uA
IO+	Driver Output Current	-	0.7	-	A
IO-	Driver Input Current	-	1.0	-	A
UV_VCC	VCC UVLO Voltage	4.0	4.8	5.5	V
HYS_VCC	VCC UVLO Hysteresis	-	0.2	-	V
UV_VBS	VBS UVLO Voltage	4.0	4.8	5.5	V
HYS_VBS	VBS UVLO Hysteresis	-	0.2	-	V
V_BSD	Bootstrap Diode Conduction Voltage Drop	-	0.7	1	V
R_BSD	Bootstrap Diode Equivalent Resistance	-	180	320	Ω

9.11 LDO Electrical Characteristics

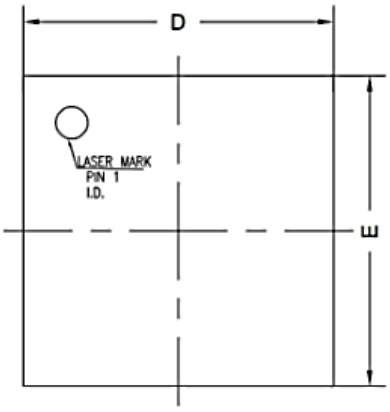
Symbol	Description	MIN	TYP	MAX	Unit
VCC12	LDO and Gate Driver Supply Voltage	5.5	-	16	V
LDO5V	LDO Output (Io=20mA, VSET is floating)	4.75	5	5.25	V
V_LineReg	LDO Linearity Rate ΔVOUT/ΔHVIN (IO=1 mA, 7.5V ≤ VCC ≤ 12.7V)	-	50		mV
V_LoadV	LDO Loading Rate ΔVOUT/ΔIOUT 1mA≤Io≤50mA	-	50		mV
V_RegDrop	LDO5V Dropping Voltage, IO=20 mA, VCC=5V	-	0.8	1.2	V
I_Lim	LDO5V Output Current Limit, VCC=12V		60-		mA

9.12 HV Buck Controller Electrical Characteristics

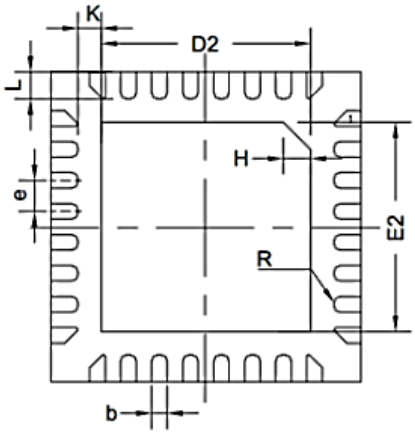
Symbol	Description	MIN	TYP	MAX	Unit
VHIN	Input Voltage	20	-	80	V
VCC12	HV-BUCK Output Voltage	12	12.5	13	V
Voc	Over-Current Detection Voltage, Voltage Difference between CS and VCC12	40	-	80	mV
Freq	Maximum Switching Frequency	-	300	-	kHz
IUG_IO+	UGATE Port Output Source Current	-	100	-	mA
IUG_IO-	UGATE Port Output Sink Current	-	200	-	mA
L	Inductance	47	-	-	uH

10. Package Information

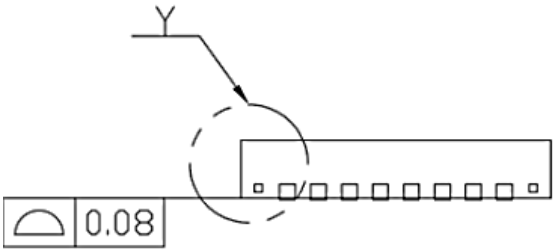
QFN-32 (4.0 x4.0 mm) Outline Dimensions



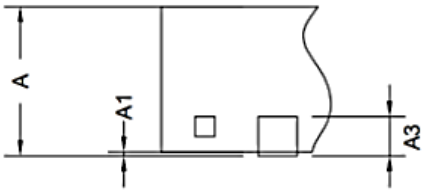
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL Y

SYMBOL	Dimension in mm		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.50	2.70	2.90
E2	2.50	2.70	2.90
K		0.30 REF	
L	0.30	0.40	0.50

Important Notice

1. inergy Technology Inc. reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

2. The Products of inergy Technology Inc. have been tested, verified and passed by our specifications and standards, and are 100% inspected before delivery from the factory. It is strongly recommended that the customers shall perform verifications of the functionality, compatibility, and reliability of the environment or platform that you used. inergy Technology Inc. would not be liable for or guarantee anything that is related to the functionality, compatibility, and reliability of the environment or platform used by the customers.